



- ☐ Tentative Specification
☒ Preliminary Specification
☐ Approval Specification

MODEL NO.: V460HK2
SUFFIX: PS5

Customer:

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

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**REVISION HISTORY**

Version	Date	Page(New)	Section	Description
Ver. 1.0	Nov 02, 2011	All	All	The preliminary specification was first issued.



1. GENERAL DESCRIPTION

1.1 OVERVIEW

V460HK2-PS5 is a 46" TFT Liquid Crystal Display product with driver ICs and 4ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 1.07G colors (8-bit+FRC).

1.2 FEATURES

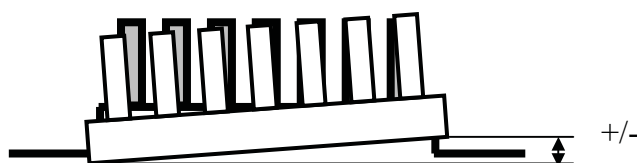
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	46
Pixels [lines]	1920 × 1080
Active Area [mm]	1018.08(H) × 572.67(V) (46" diagonal)
Sub-Pixel Pitch [mm]	0.17675(H) × 0.53025(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 2445g
Physical Size [mm]	1047.76(W) × 625.82(H) × 1.78(D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	5000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR ≥ 20) (Typical value measure at CMI's module)
Color Chromaticity	* Please refer to "color chromaticity" on p.32
Cell Transparency [%]	6.2%
Polarizer Surface Treatment	Anti-Glare coating (Haze 3.5%), Hard coating (H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	2395	2445	2495	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm 0.5\text{mm}$ as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1) With CMI Module
Operating Ambient Temperature	TOP	0	50	°C	(1), (2) With CMI Module

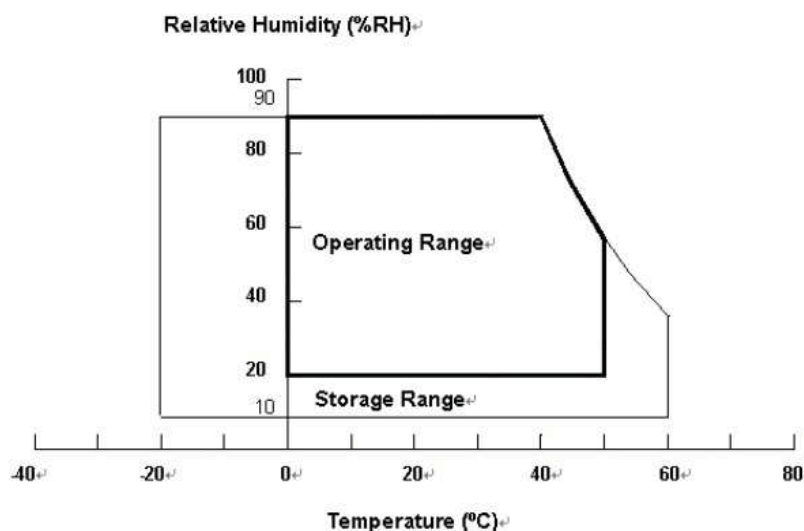
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



**2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)**

Storage Condition: With shipping package.

Storage temperature range: 25 ± 5 °CStorage humidity range: $50 \pm 10\%$ RH

Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS**2.3.1 TFT LCD OPEN CELL**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

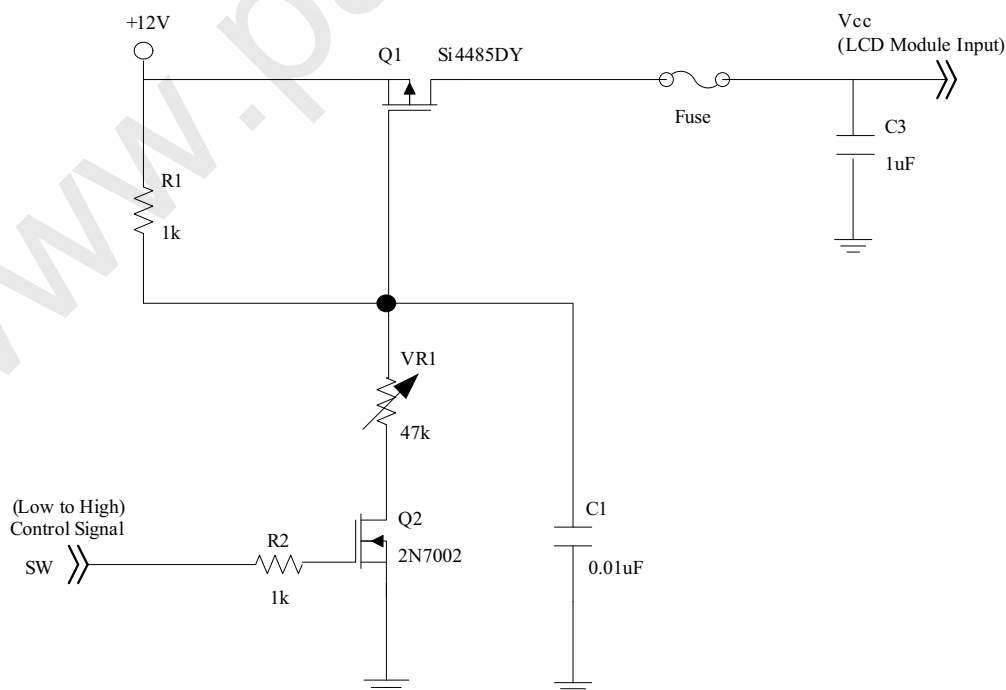
3.1 TFT LCD OPEN CELL

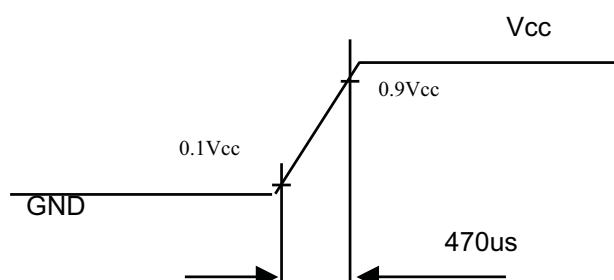
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	3.0	A	(2)
Power Supply Current	White Pattern	—	—	0.66	0.79	A	(3)
	Horizontal Stripe	—	—	1.49	1.83	A	
	Black Pattern	—	—	0.64	0.77	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

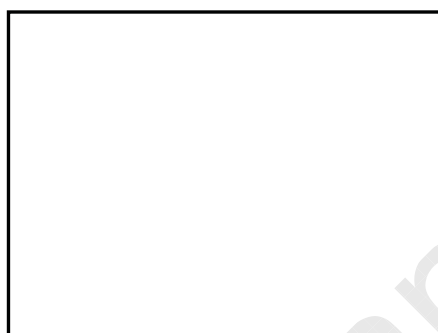
Note (2) Measurement condition:



Vcc rising time is 470us

Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



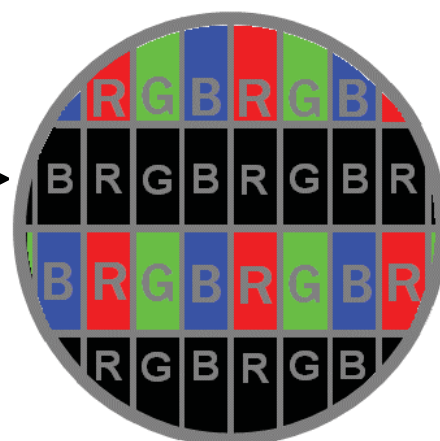
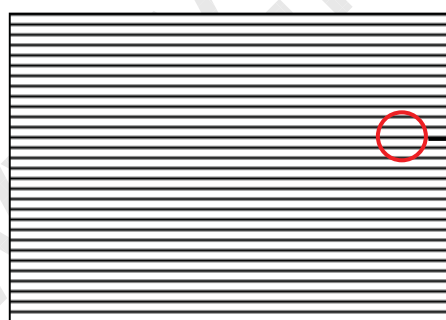
Active Area

b. Black Pattern

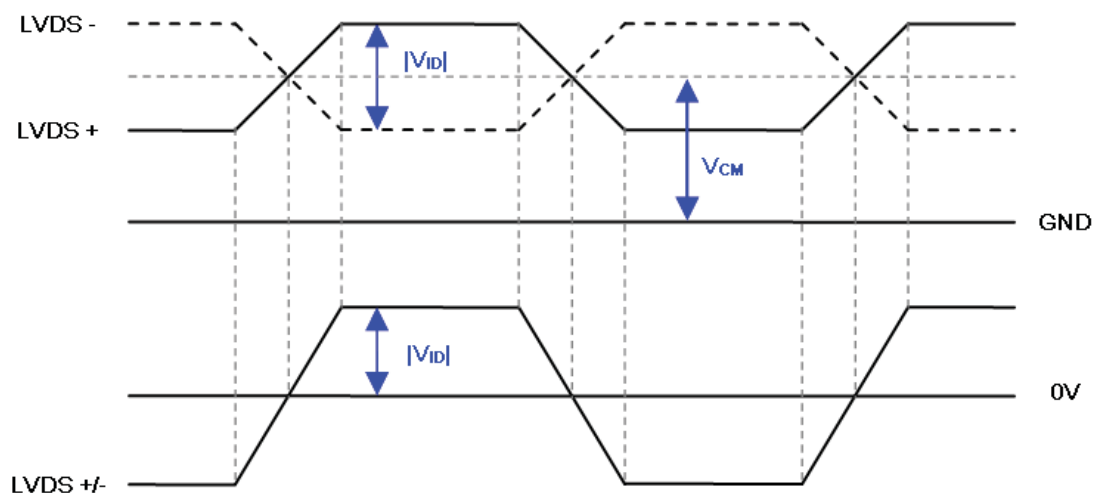


Active Area

c. Horizontal Stripe Pattern

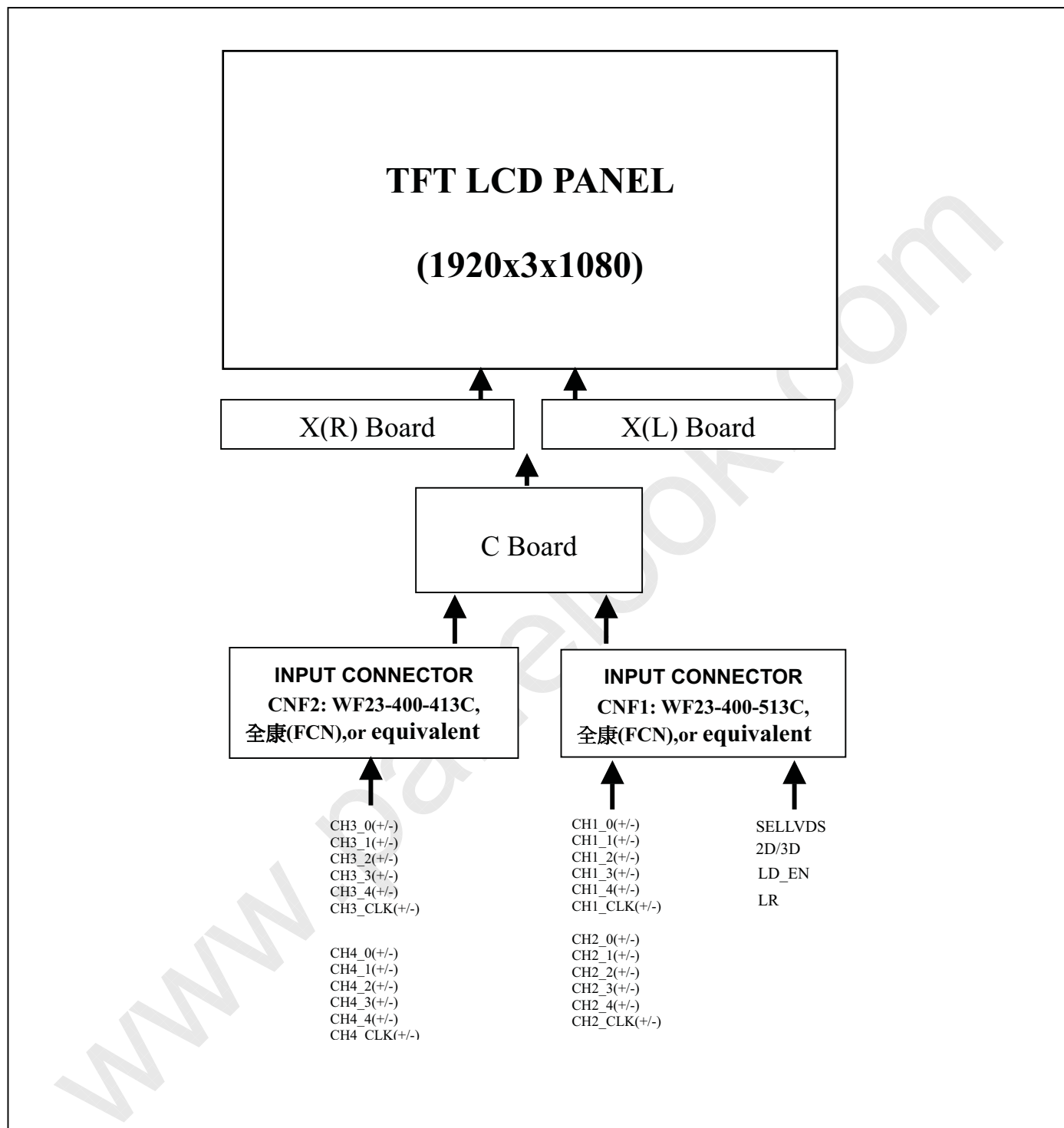


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



**5. INPUT TERMINAL PIN ASSIGNMENT****5.1 TFT LCD Module Input**

CNF1 Connector Pin Assignment: (WF23-400-513C,全康(FCN),or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	EEPROM Serial Clock (for local dimming demo function)	(11)
3	SDA	EEPROM Serial Data (for local dimming demo function)	
4	N.C.	No Connection	(1)
5	L/R_O	Output signal for Left Right Glasses control	(10)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)(7)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	(9)
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	(9)
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	(9)
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(6)(8)
27	L/R	Input signal for Left Right eye frame synchronous	(4)(8)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	(9)



29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	(9)
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	(9)
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	LD_EN	Input signal for Local Dimming Enable	(5)(7)
43	SCN_EN	Input signal for Scanning Enable	(6)(8)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	



CNF2 Connector Pin Assignment (WF23-400-413C,全康(FCN),or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	(9)
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	(9)
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	(9)
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	GND	Ground	
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	(9)
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	



31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	(9)
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	(9)
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	GND	Ground	
41	GND	Ground	

CN6 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(10)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or Open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

$V_{IL}=0\sim 0.8\text{ V}$, $V_{IH}=2.0\sim 3.3\text{ V}$

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) Local dimming enable selection.

L= Connect to GND, H=Connect to +3.3V or Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

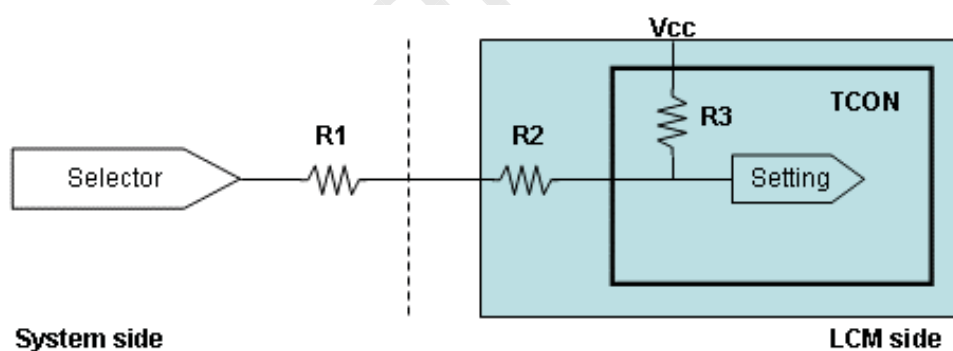
Note (6) Scanning enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

SCN_EN	Note
L or Open	Scanning Disable
H	Scanning Enable

Note (7) SELLVDS, LD_EN signal pin connected to the LCM side has the following diagram.

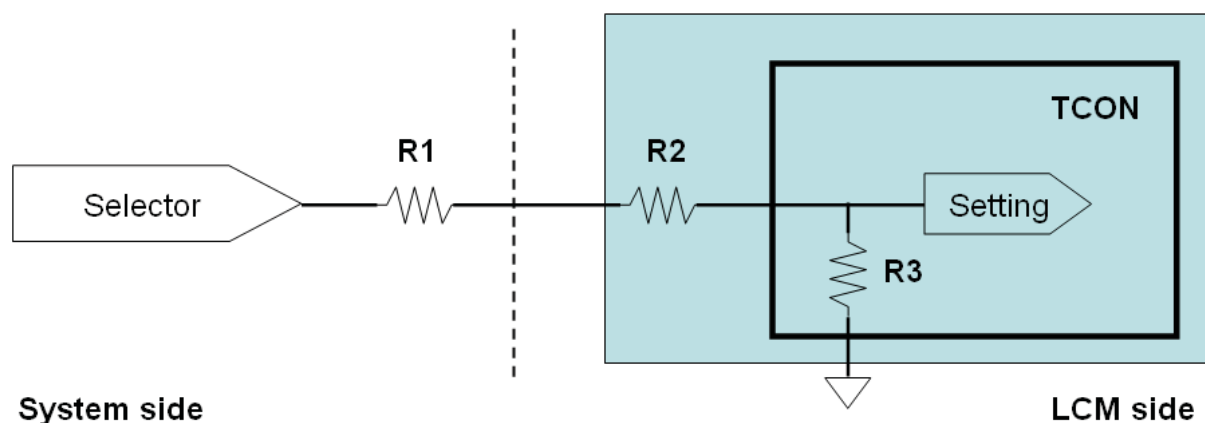
R1 in the system side should be less than 1K Ohm. ($R1 < 1K\text{ Ohm}$)



System side
 $R1 < 1K$

Note (8) 2D/3D, L/R and SCN_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ($R1 < 1K\text{ Ohm}$)



System side: $R1 < 1K$

Note (9) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9,1913, 1917
2nd Port	Second Pixel	2, 6, 10,1914, 1918
3rd Port	Third Pixel	3, 7, 11,1915, 1919
4th Port	Fourth Pixel	4, 8, 12,1916, 1920

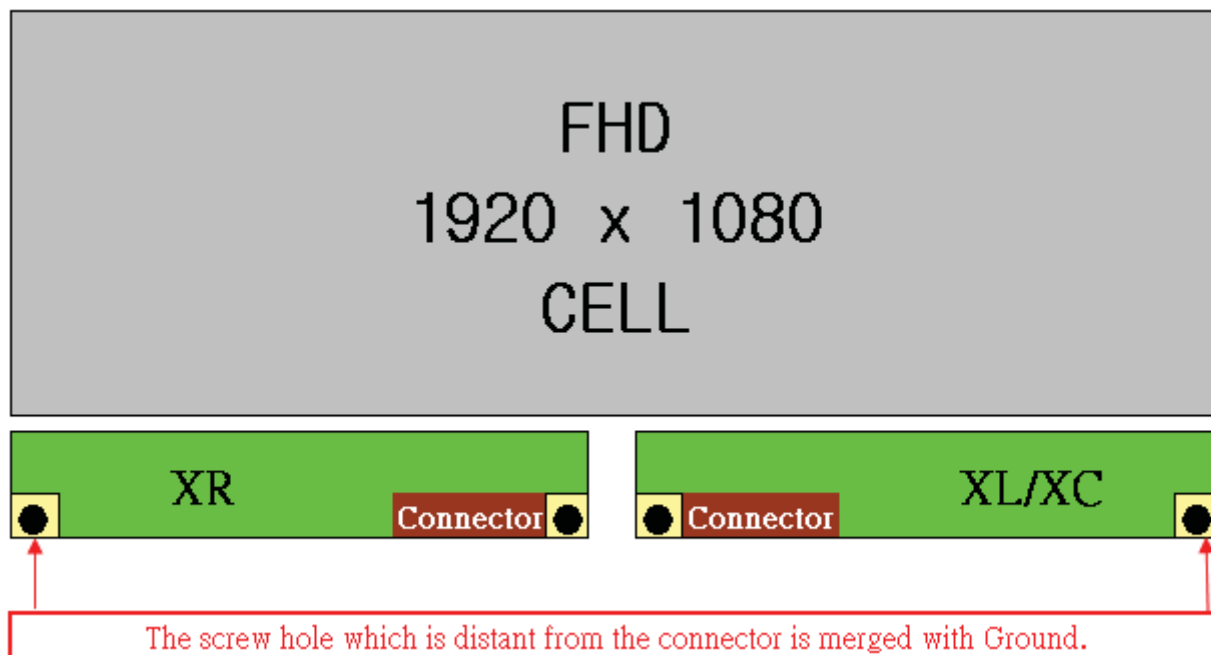
Note (10) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

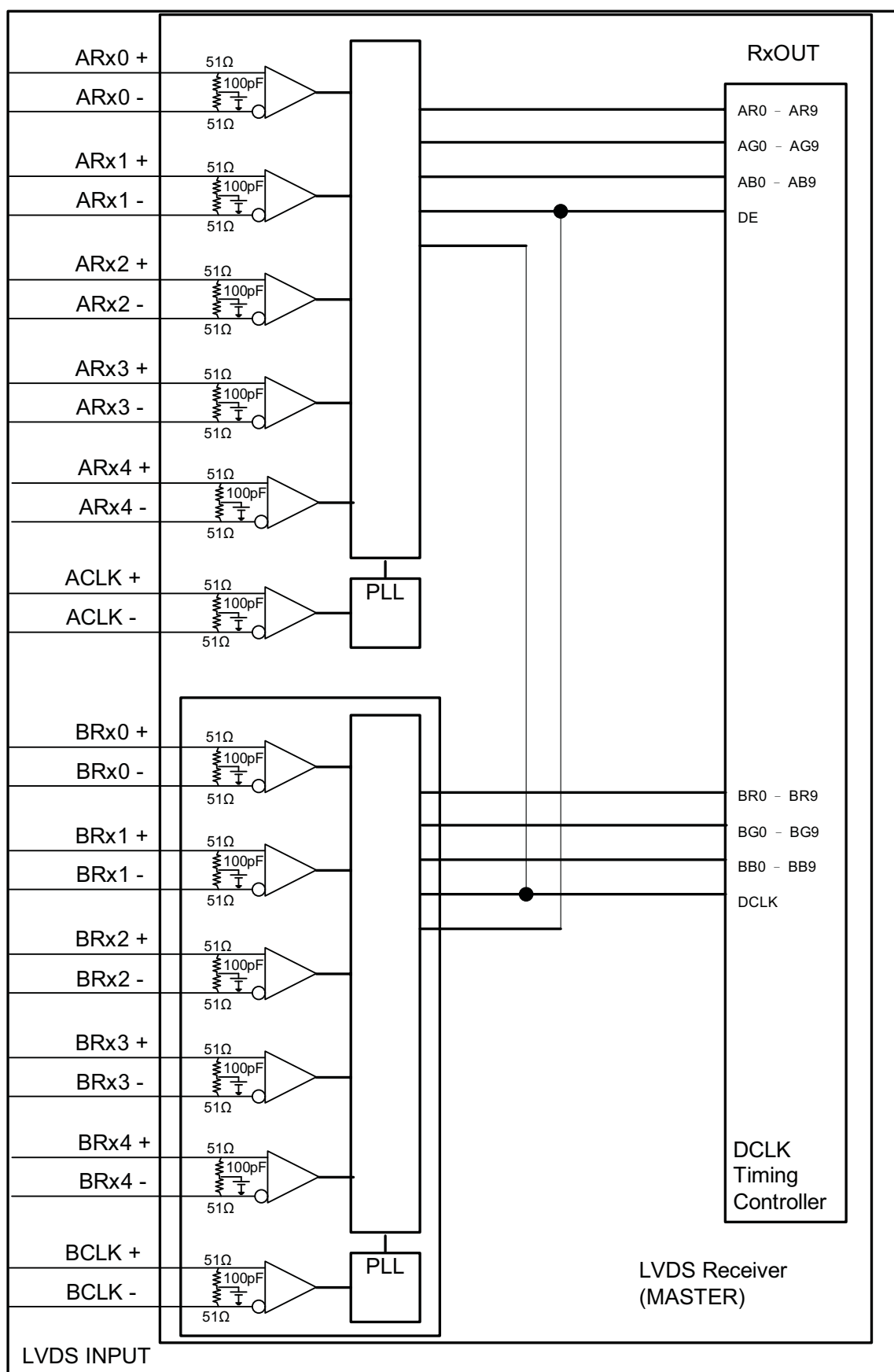
L/R_O	Note
L	Right glass turn on
H	Left glass turn on

Note (11) Please reference Appendix A

Note (12) The screw hole which is distant from the connector is merged with Ground



5.2 BLOCK DIAGRAM OF INTERFACE





AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

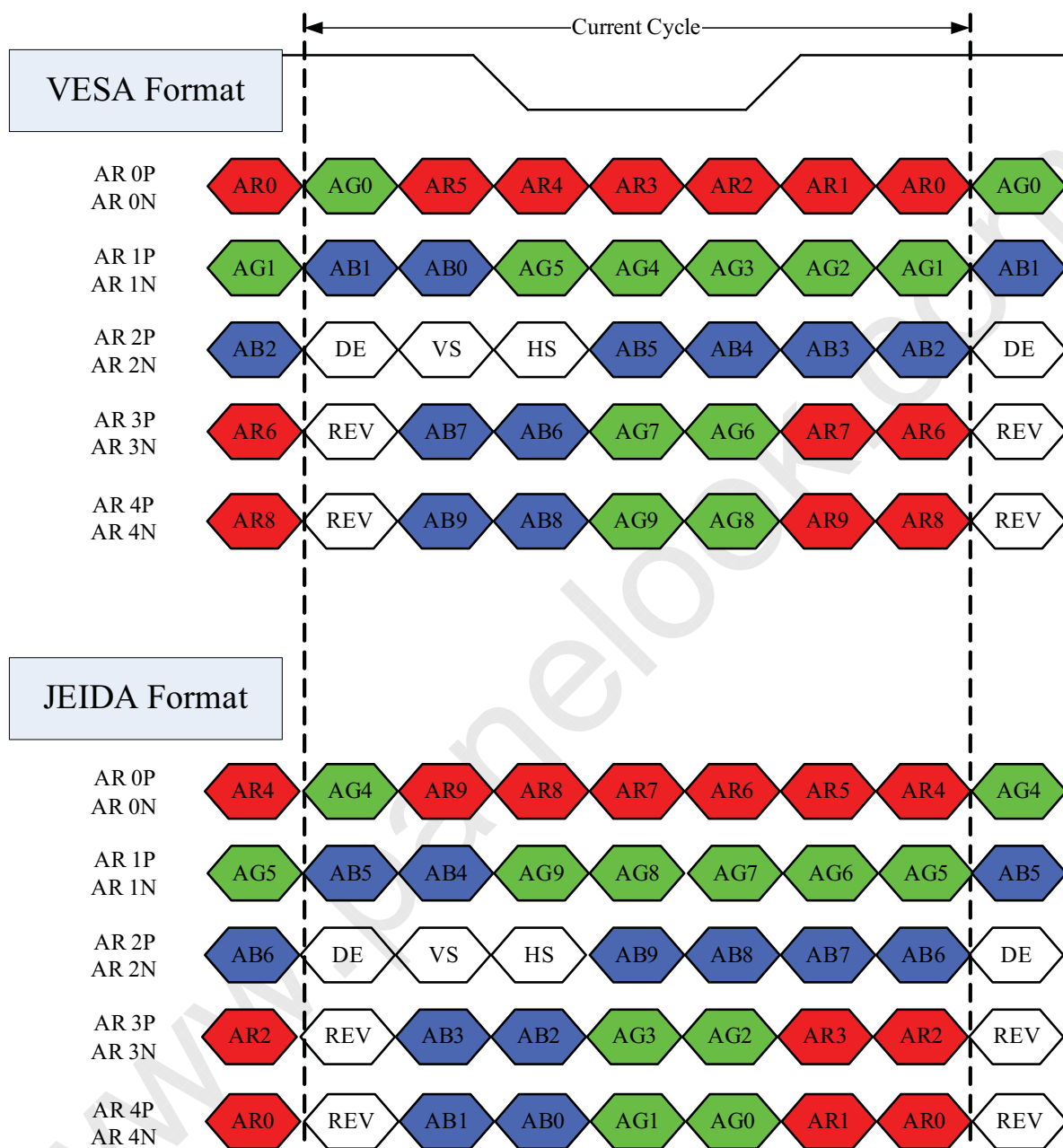
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.3 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSV: Reserved

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																												
		Red										Green										Blue								
R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0



PRODUCT SPECIFICATION

	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
--	-------------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

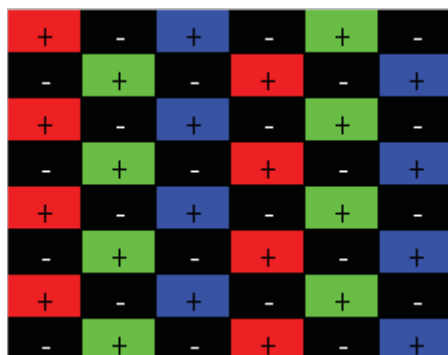
Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 FLICKER (Vcom) ADJUSTMENT

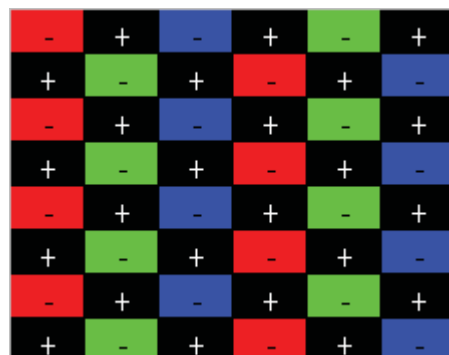
(1) Adjustment Pattern:

Flick pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

. Frame N



Frame N+1



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

- USB Sensor Board.
- Programmable software.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-2\%$	-	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	-	-	ps	(5)
	Hold Time	T_{lvhd}	600	-	-	ps	

6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	
	3D mode		F_{r5}	100	100	100	Hz	(7)
Vertical Active Display Term	2D Mode	Total	T_{v}	1090	1350	1395	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
		Display	T_{vd}	1080	1080	1080	Th	—
		Blank	T_{vb}	10	270	315	Th	—
	3D Mode	Total	T_{v}	1350			Th	(6)(8)
		Display	T_{vd}	1080			Th	
		Blank	T_{vb}	270			Th	
Horizontal Active Display Term	2D Mode	Total	T_{h}	520	550	670	T_{c}	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
		Display	T_{hd}	480	480	480	T_{c}	—
		Blank	T_{hb}	40	70	190	T_{c}	—
	3D Mode	Total	T_{h}	520	550	670	T_{c}	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
		Display	T_{hd}	480	480	480	T_{c}	—
		Blank	T_{hb}	40	70	190	T_{c}	—

6.1.2 Timing spec for Frame Rate = 120Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	114	120	126	Hz	
	3D mode		F_{r6}	120	120	120	Hz	(7)
Vertical Active Display Term	2D Mode	Total	T_v	1090	1125	1395	T_h	$T_v = T_{vd} + T_{vb}$
		Display	T_{vd}	1080	1080	1080	T_h	—
		Blank	T_{vb}	10	45	315	T_h	—
	3D Mode	Total	T_v	1125			T_h	(6)(8)
		Display	T_{vd}	1080			T_h	
		Blank	T_{vb}	45			T_h	
Horizontal Active Display Term	2D Mode	Total	T_h	520	550	670	T_c	$T_h = T_{hd} + T_{hb}$
		Display	T_{hd}	480	480	480	T_c	—
		Blank	T_{hb}	40	70	190	T_c	—
	3D Mode	Total	T_h	520	550	670	T_c	$T_h = T_{hd} + T_{hb}$
		Display	T_{hd}	480	480	480	T_c	—
		Blank	T_{hb}	40	70	190	T_c	—

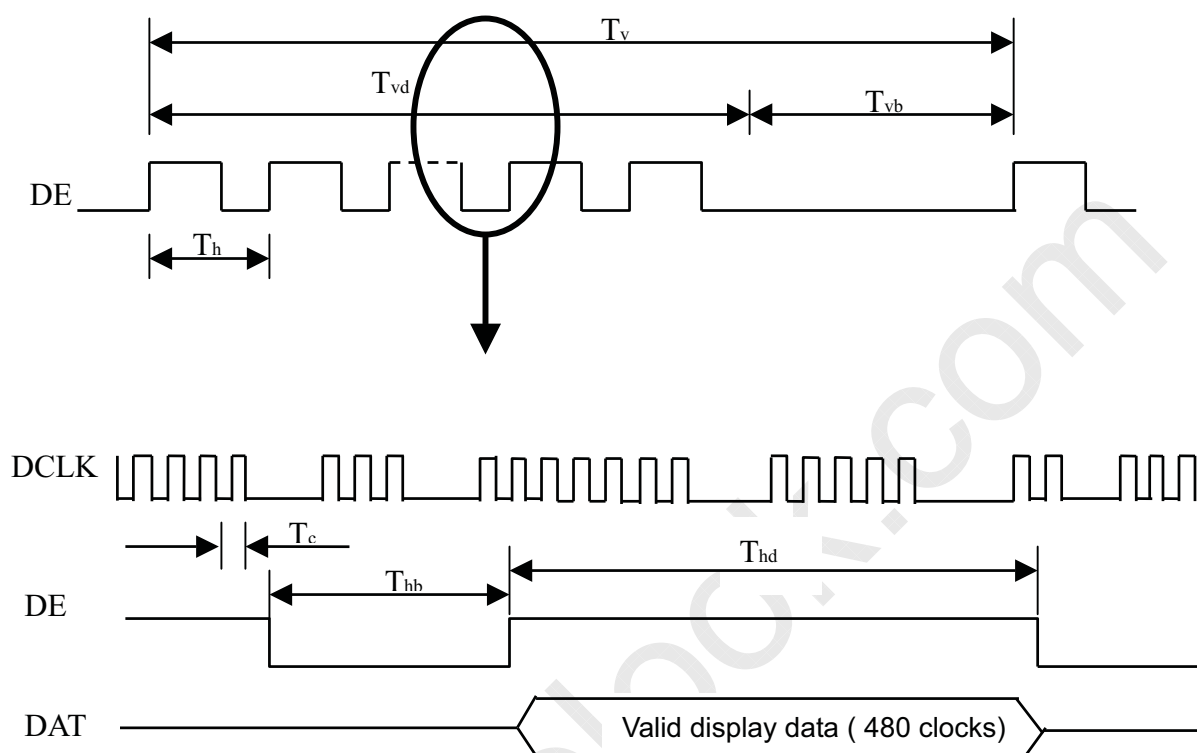
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

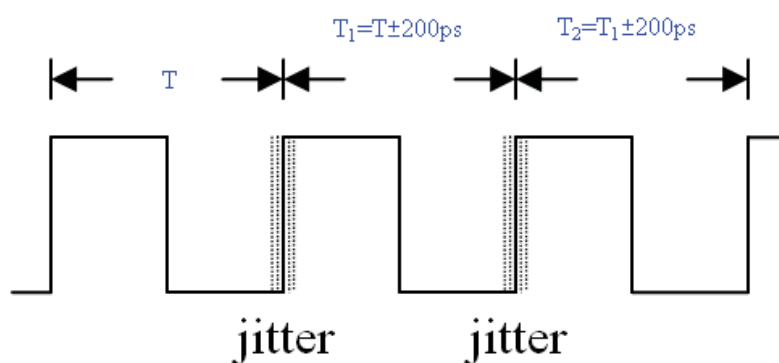
$$F_{clk}(max) \geq F_{r6} \times T_v \times T_h$$

$$F_{r5} \times T_v \times T_h \geq F_{clk}(min)$$

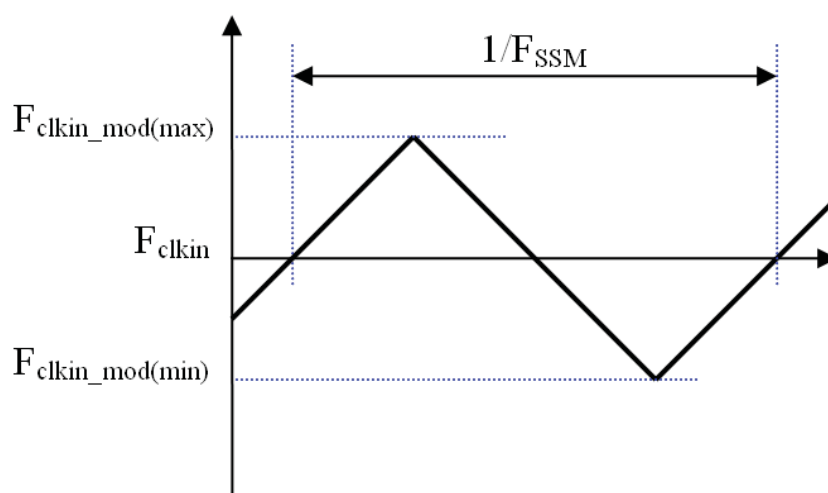
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_2|$

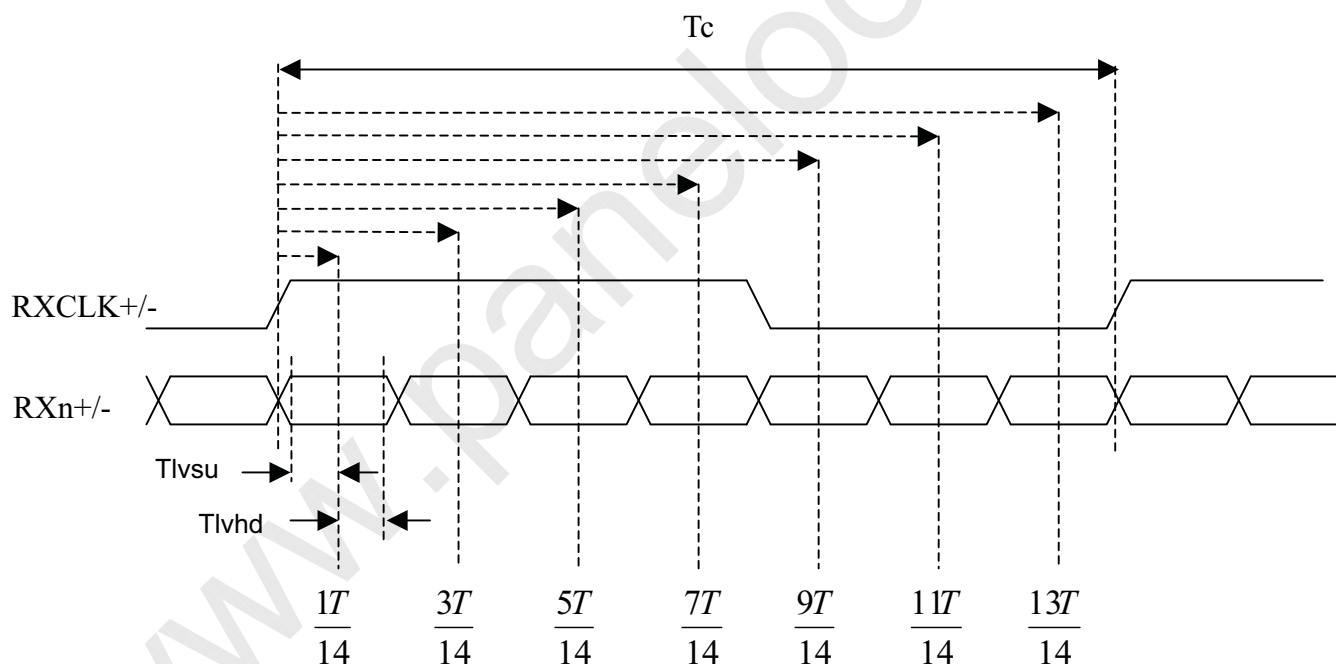


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 100Hz 3D mode
and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 120Hz 3D mode

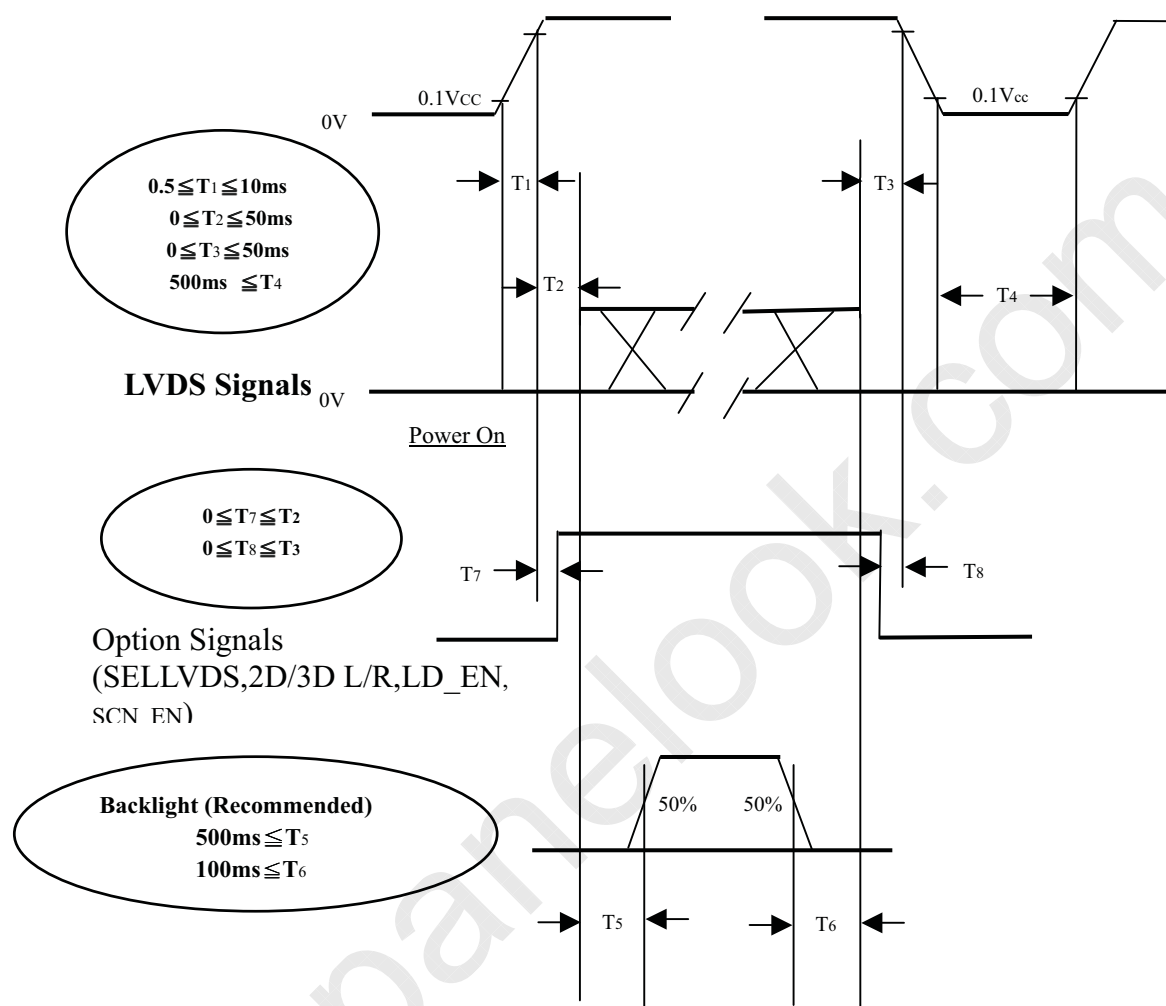
Note (7) In 3D mode, the set up Fr5 and Fr6 in Typ. ± 3 HZ .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ. ± 30 .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

6.2 POWER ON/OFF SEQUENCE

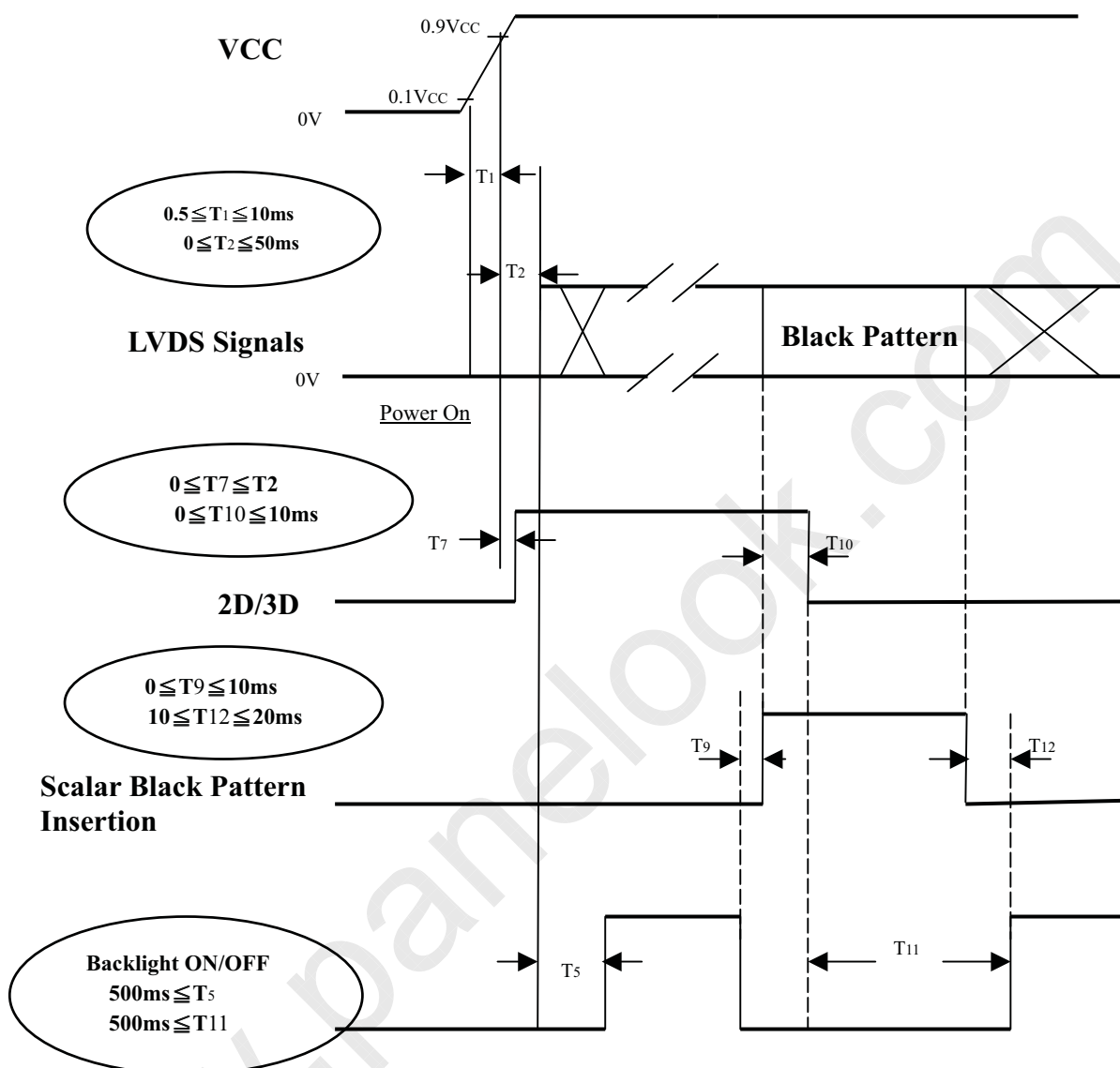
6.2.1 POWER ON/OFF SEQUENCE($T_a = 25 \pm 2^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.2.2 D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of V_{cc}.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{cc} is in off level, please keep the level of input signals on the low or high impedance. If T₂<0, that maybe cause electrical overstress failure.

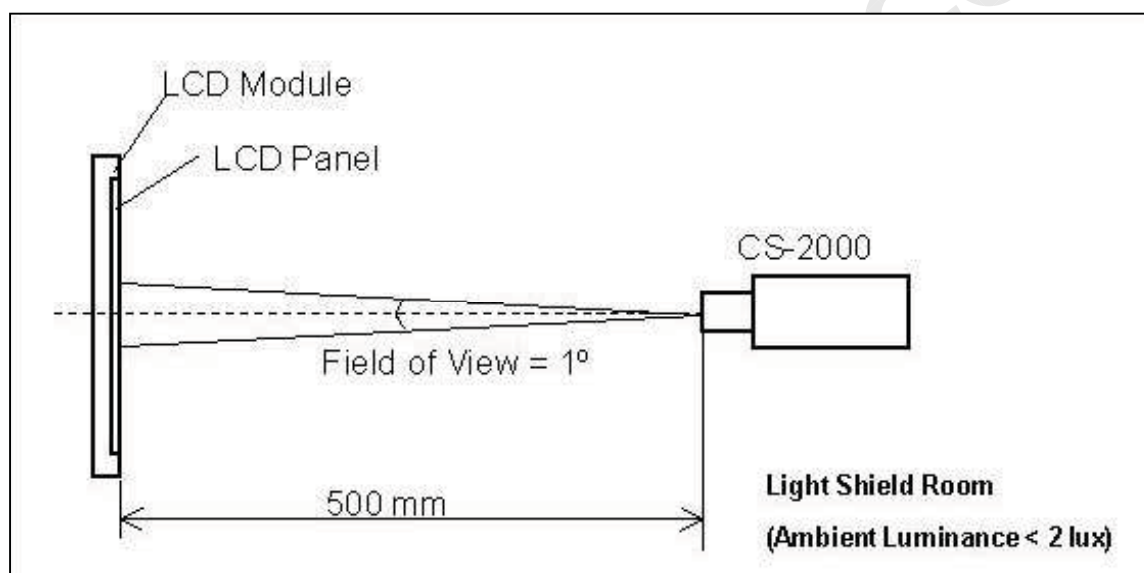
Note (4) T₄ should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	130	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Angle at Normal Direction Standard light source “C”	-	0.654	-	-	(0)
		Rcy			0.329		-	
	Green	Gcx			0.275		-	
		Gcy			0.600		-	
	Blue	Bcx			0.147		-	
		Bcy			0.106		-	
	White	Wcx			0.320		-	
		Wcy			0.365		-	
Center Transmittance		T%	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI module	-	6.1	-	%	(1),(6)
Contrast Ratio		CR			800	-	-	(1),(3)
Response Time		Gray to gray	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI Module@60Hz	-	6.5	12		(1),(4)
White Variation		δW	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI module	-	-	1.3	-	(1),(5)
Viewing Angle	Horizontal	θ_x^+	$CR\geq 20$ With CMO module		88		Deg.	(1),(2)
		θ_x^-			88			
	Vertical	θ_Y^+			88			
		θ_Y^-			88			
Transmission direction of the up polarizer		Φ_{up-P}	-	-	90(VA) 135(TN)	-	Deg.	(7)
slow axis of the QWP		Φ_{up-Q}	-	-	135(VA) 180(TN)	-	Deg.	(7)

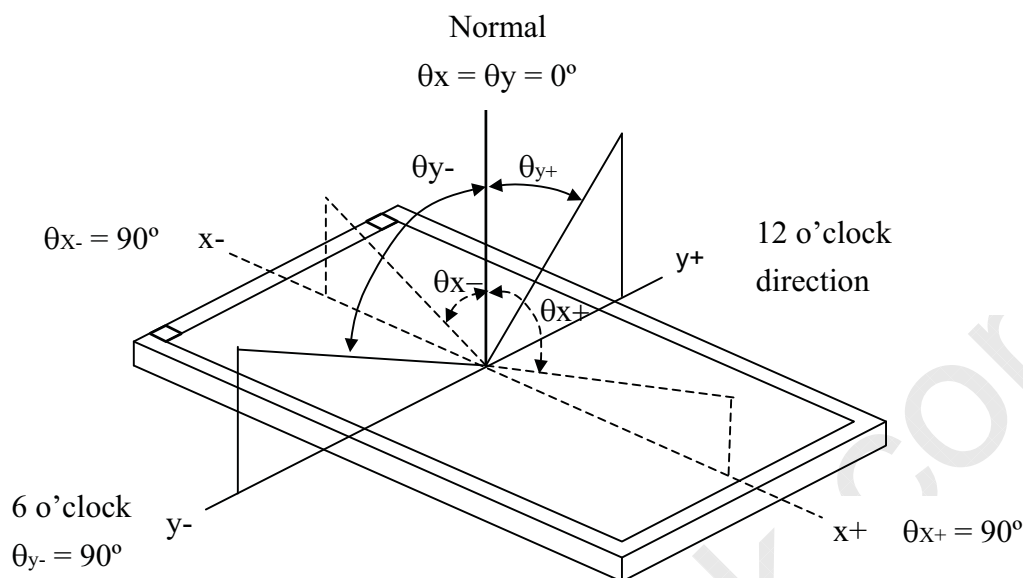
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum at center point. White is without signal input and R,G,B are with signal input. BLU (for V460HK2-PS5) is supplied by CMO.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θ_x , θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

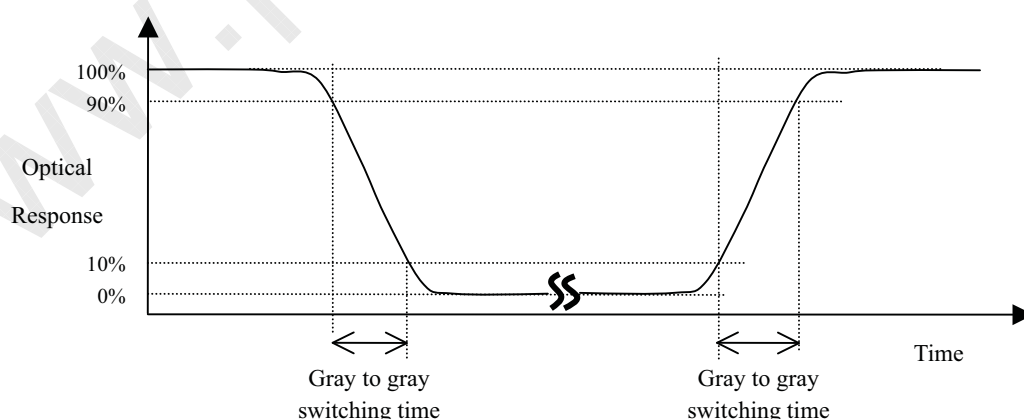
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Gray-to-Gray Switching Time: (VA case)



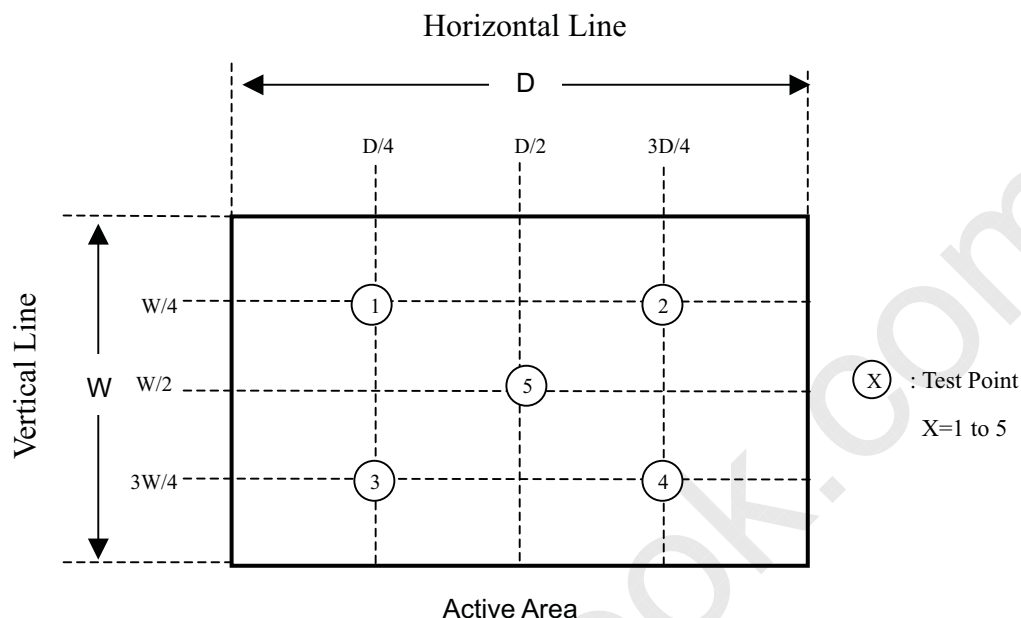
The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



Note (6) Definition of Transmittance (T%) :

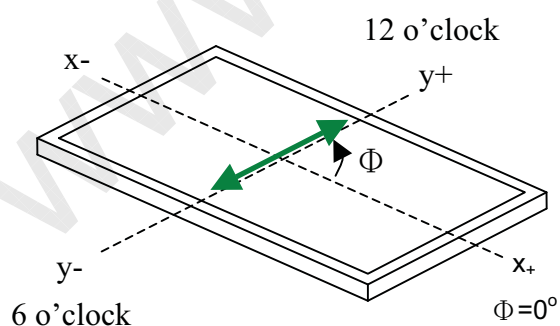
Measure the luminance of gray level 255 at 5 points of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{average [L (1), L (2), L (3), L (4), L (5)] of LCD module}}{\text{average [L (1), L (2), L (3), L (4), L (5)] of backligh unit}} \times 100\%$$

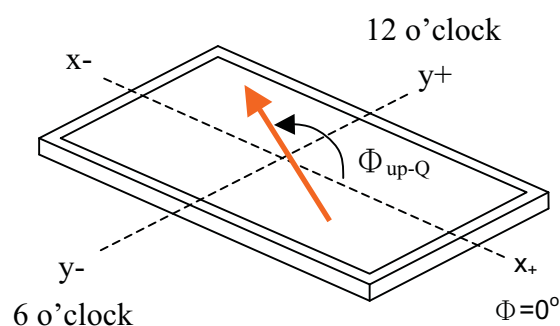
The 5 point is corresponding of the point X at the figure in Note (5).

Note (7) This is a reference for designing the shutter glasses of 3D application.

Definition of the transmission direction of the up polarizer ($\Phi_{\text{up-P}}$) and the slow axis of QWP ($\Phi_{\text{up-Q}}$) on LCD Module:

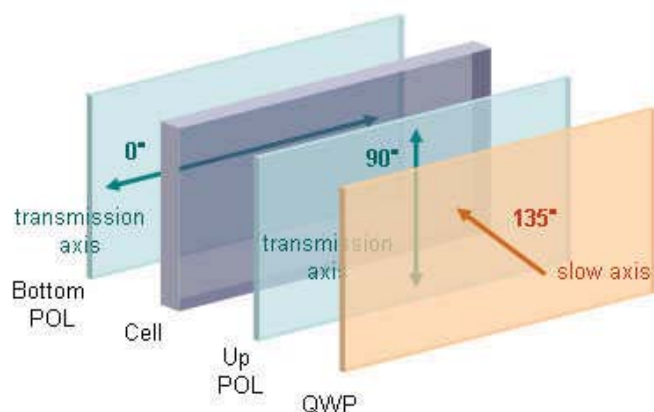


Up Polarizer

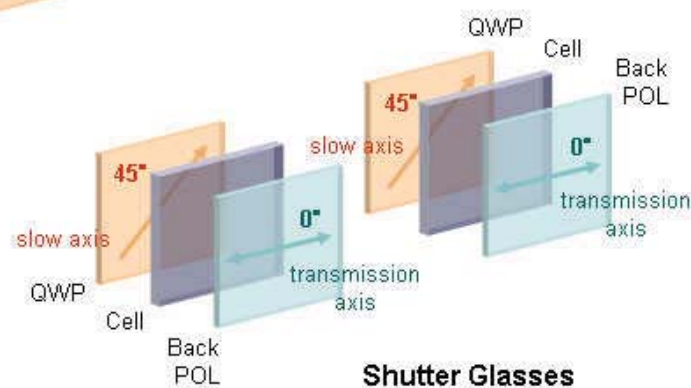


QWP

The slow axis of the QWP on shutter glasses should be perpendicular to the QWP on LCD Module to get better 3D performance.



LCD Module



Shutter Glasses

8.0 DEFINITION OF LABELS

8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

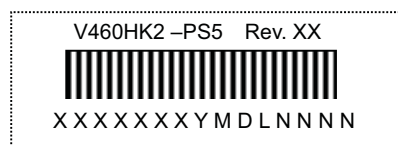
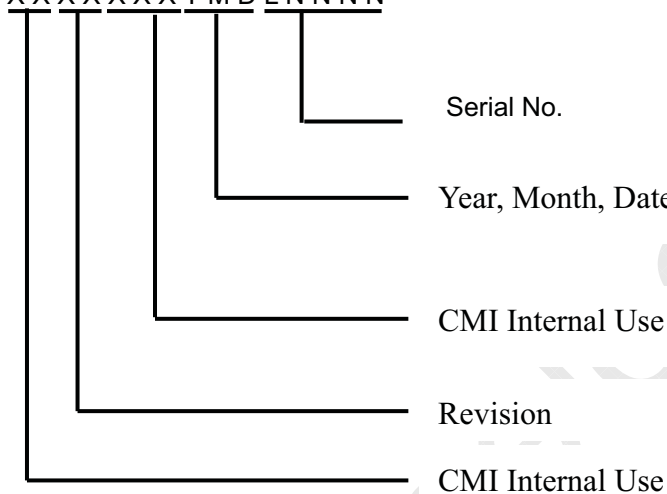


Figure.8-1 Serial No. Label on SPWB

Model Name: V460HK2-PS5

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2...etc.

Month: 1~9, A~C, for Jan. ~ Dec.


Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

8.2 CARTON LABEL

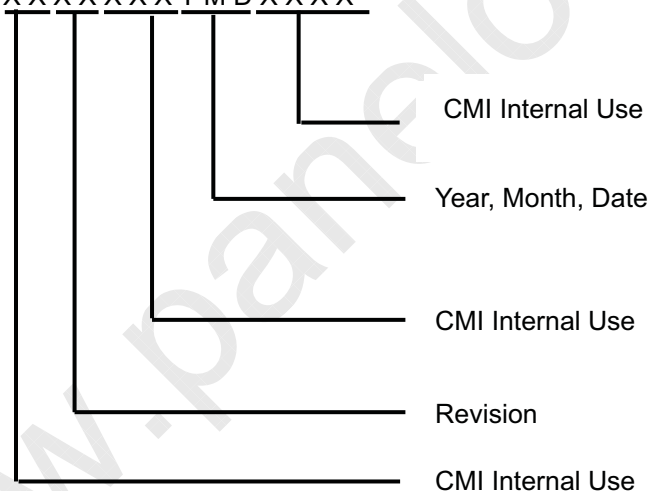
The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

P.O. NO.	_____ Made In Taiwan (Made In China)	
Part ID.	_____	Quantities _____
Model Name	_____ V460HK2-PS5	Rev. _____
Carton ID.	 XXXXXXXYMDXXXX	RoHS

Carton label includes the information as below:

(a) Model Name: V460HK2- PS5

(b) Carton ID: X X X X X X Y M D X X X X



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2...etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

(c) Quantities: 8

9. PACKAGING

9.1 packing specifications

- (1) 8 LCD TV Panels / 1 Box
- (2) Box dimensions : 1260 (L) X960 (W) X99 (H)mm
- (3) Weight : approximately 33Kg (8 panels per box)
- (4) 96 LCD TV Panels / 1 Group

9.2 packing Method

Figures 9-1 and 9-2 are the packing method

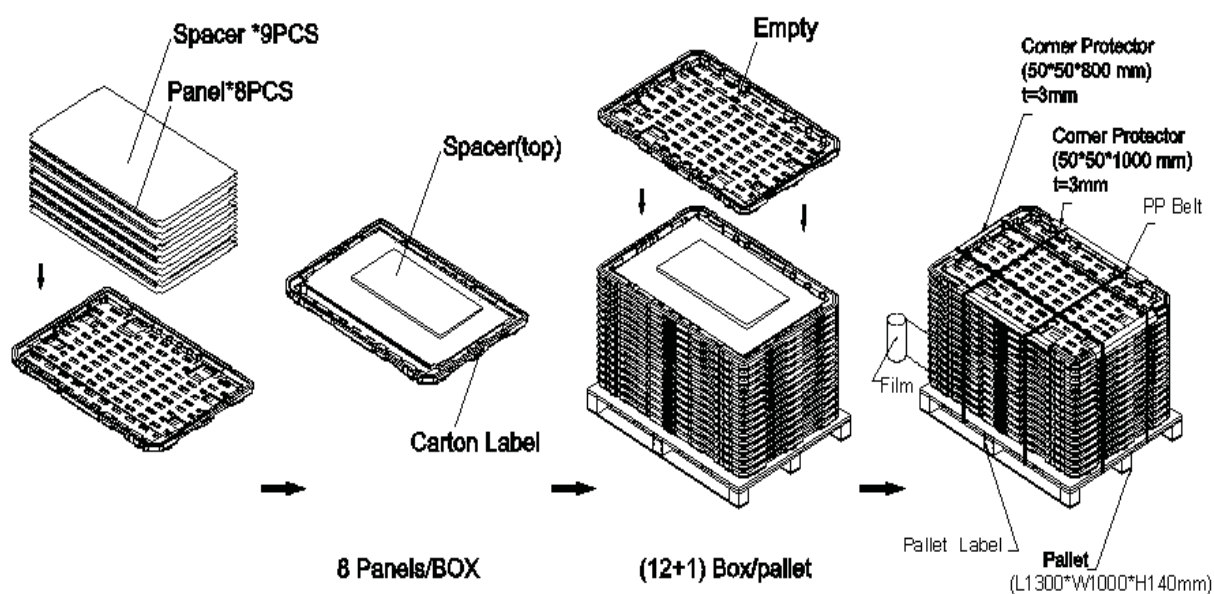
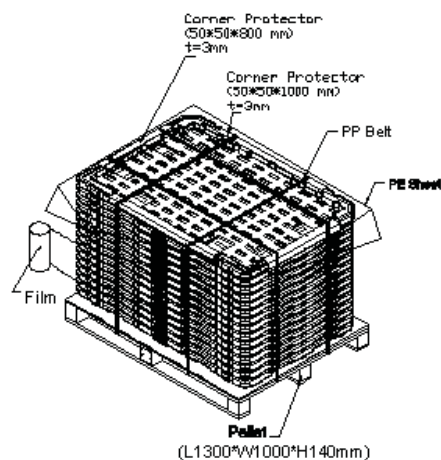


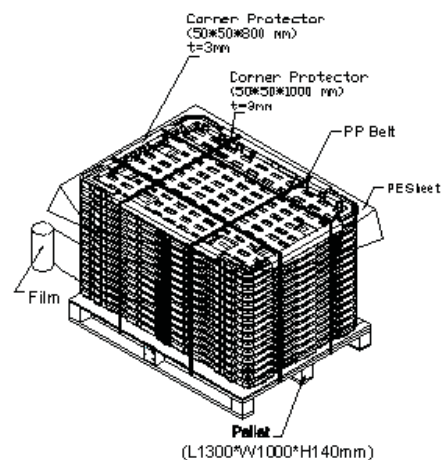
Figure.9-1 packing method

Sea / Land Transportation

Air Transportation



{12+1} Box/pallet



{12+1} Box/pallet

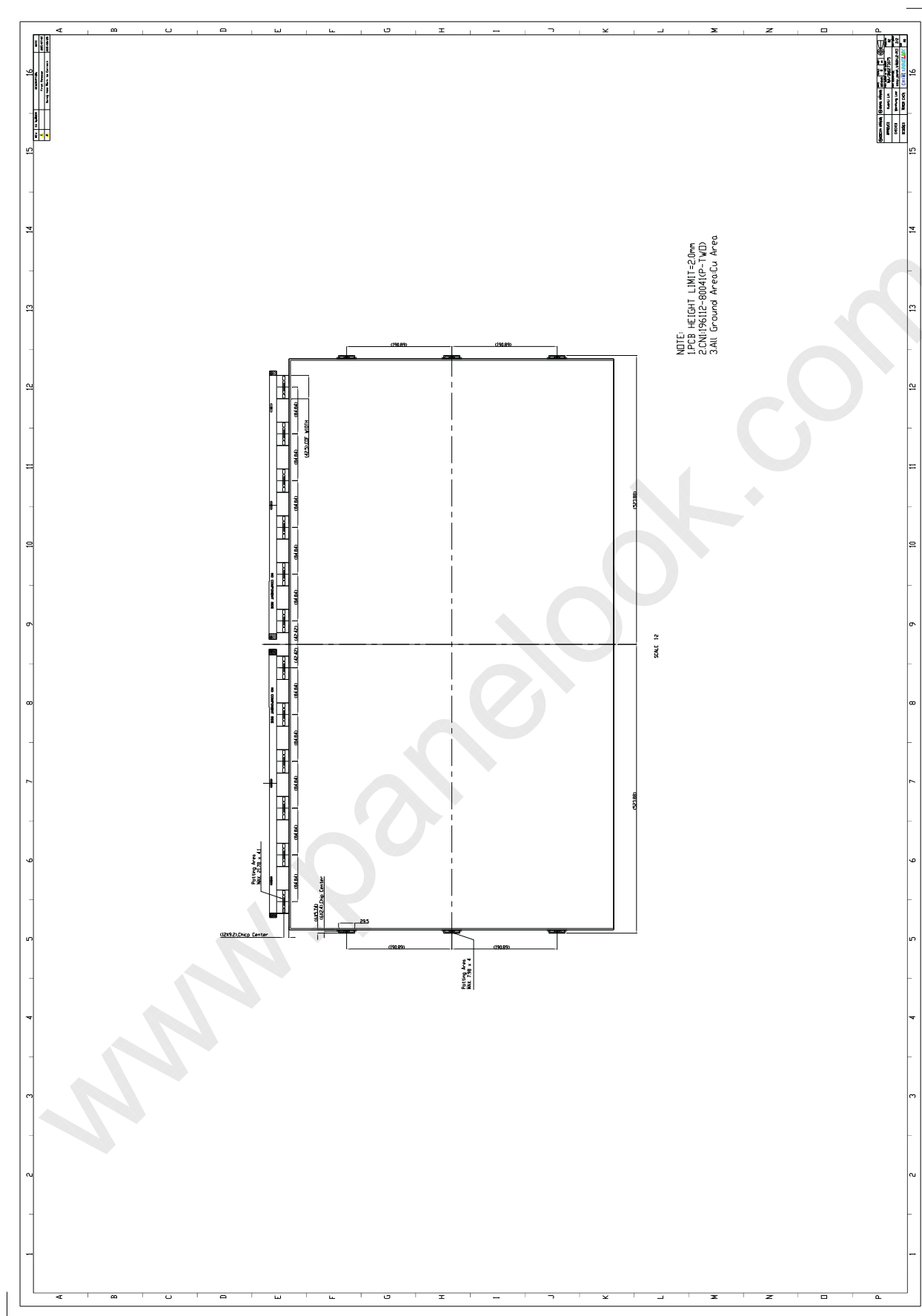
Figure.9-2 packing method

10. PRECAUTIONS**10.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) Do not apply rough force such as bending or twisting to the product during assembly.
- (2) To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.
- (4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.
- (8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.
- (9) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

- (1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (2) After the product's end of life, it is not harmful in case of normal operation and storage.





APPENDIX 1: PANEL MODULE DESIGN AND MANUFACTURE REFERENCE GUIDE

A.1 FFC CONNECTOR

A.2 PCBA GROUNDING

A.3 LCM ASSEMBLY GUIDELINE

ELINE